Fermilab

CIA Dataway Controller EPLD

20 March 1997, P. Kasley

Registers

Address Register (R/W)

A2=0, A1=0

15	14	13..12	11	10	9	8	7..4	3	2	1	0
A	R		MS 3	MS 2	MS 1	MS 0		AS 3	AS 2	AS 1	AS 0

MS[3..0] Module Select, 0-15
AS[3..0] Module sub-address, 0-15

A	R	Operation
0	0	digital write cycle
0	1	digital read cycle
1	0	not used
1	1	analog read cycle

Data Register (R/W)

A2=0, A1=1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	0	0	0	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

ERR: Set for all error conditions. Reset by writing to the Status Register.

Bits 0-7 are used for digital reads and writes. Bits 0-11 return ADC data.

Status Register (R/W)

A2=1, A1=0

15	14..3	2	1	0
DRDY		DWO	NACK	ATO

DRDY: Dataway ready. Set upon completion of a dataway cycle. Reset by writing to the address register. For digital and analog read cycles, DRDY indicates that the data and status registers are valid. For digital write cycles, DRDY indicates that the write cycle completed and the status register is valid.

ATO: ADC timeout. Set if an analog read dataway cycle is aborted. Reset by writing to the Status Register

NACK: Module negative acknowledge. Set if the selected module fails to respond to a dataway cycle. Reset by writing to the Status Register.

DWO: Dataway overlap. Set when the processor attempts to write to any register while a dataway cycle is in progress. Reset by writing to the Status Register. *CAUTION! The address and data registers are locked during the cycle. The status and control registers are not and will be corrupted by an errant write cycle.*

Control Register (R/W)
A2=1, A1=1

15	14	13	12..0
AIE	DIE	SMR	

AIE: Analog Interrupt Enable. If set, the processor will be interrupted when DRDY goes active after an analog read cycle
DIE: Digital Interrupt Enable. If set, the processor will be interrupted when DRDY goes active after a digital read or write cycle.
SMR: State Machine Reset. If set, the dataway cycle controller is reset to the idle state. Reset is held until SMR is reset.

Operation

Digital Write Cycle:
1. Write data to the low byte of the data register.
2. Write module select, address, and cycle type to address register.
3. Poll the status register for DRDY or "wait" for DRDY interrupt.
4. Check status for errors.

Digital Read Cycle:
1. Write module select, address, and cycle type to address register.
2. Poll the status register for DRDY or "wait" for DRDY interrupt.
3. Read the data register.
4. Check status register if error flag is set.

Analog Read Cycle:
1. Write module select, address, and cycle type to address register.
2. Poll the status register for DRDY or "wait" for DRDY interrupt.
3. Read the data register.
4. Check status register if error flag is set.

The Dataway Controller holds its interrupt line active until the status register is read.

DWC Pinout (MAX7128 EPLD, 84 lead PLCC)
Note: Pin 84 must connect to pin 62, and pin 2 must connect to pin 23 for proper operation

Name	I/O	Description	Nr
CPU Signals			
D[0..15]	I/O	Bidirectional CPU data	40,39,37,28,54,30,31,27,57,55,60,58,67,63,56,36
/RD	In	CPU read strobe	8
/WR	In	CPU write strobe	11
/CS	In	CPU chip select	6
LA1,LA2	In	CPU address	12,10
IRQ	Out	Interrupt request: driven high at the end of a dataway cycle to signal the CPU.	33
Dataway Signals			
CD[0..7]	I/O	Bidirectional dataway data	41,15,14,29,18,21,22,34
CDDIR	Out	Dataway data direction control. An external buffer can be enabled to drive from the dataway to CD[0..7] when CDDIR is low.	61
/ACK	In	Dataway module acknowledge	9
/A	Out	Dataway analog operaton select	46
/R	Out	Dataway read operation select	44
/AS[0..3]	Out	Dataway module sub-address	35,17,16,25
MS[0..3]	Out	Binary-encoded module select	50,45,49,48
/MSE	Out	Module select enable: used with MS[0..3] to generate sixteen unique dataway module selects.	64
ADC Control Signals			
/CNVT	Out	AD1674 R/C input: pulses low to start a conversion.	81
STS	In	AD1674 status output: goes high while the AD1674 performs a conversion.	5
/ADCOE	Out	ADC output enable: enables an external buffer to gate the AD1674 data lines onto the CPU data bus.	24
ERR	Out	Dataway error status: gated onto D15 of the	4

		CPU data bus by /ADCOE to provide error status for ADC data reads	
Utility Signals			
/DIG_WR	Out	Active during a digital write cycle.	51
/DIG_RD	Out	Active during a digital read cycle.	52
/ANA_RD	Out	Active during an analog read cycle.	73
CLK	In	10 Mhz clock	83
/RST	In	Master reset	1
Power Connections			
Vcc	5V	3,13,26,38,43,53,66,78	
Gnd	0V	7,19,32,42,47,59,72,82	